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A Measurement Method for the Increase of Digital Switching Time Due to Hot-Electron Stress

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Abstract—**Channel hot-electron (CHE) injection poses a reliability problem for n-channel field-effect transistors with small design rules. One often assesses the reliability of a particular fabrication process and design by subjecting individual transistors, instead of an entire circuit, to continuous or pulsed voltage stress. Simple inspection of the linear region transconductance degradation and threshold voltage shift of the individual devices, however, does not yield direct information on the circuit performance impact of channel hot-electron stress. In this letter we describe a simple measurement method for the extraction of the increase of digital switching time due to channel hot-electron stress. One performs this measurement on discrete transistors so that reliability tests still employ these individual devices. We obtain good agreement between this method and a direct measurement of the increased switching time of a CMOS inverter. We also find that the switching time changes negligibly even when the linear transistor characteristics are severely degraded if this switching delay is measured with the same source and drain terminals as were employed for the hot-electron stress.**

AS IS WELL KNOWN, channel hot-electron (CHE) injection poses an obstacle for miniaturization of NMOS FET's [1], [2]. A common method of qualifying an existing NMOS or CMOS technology for CHE stability is to place discrete FET's under dc stress ($V_{ds} = V_{dd} - V_{ss}$ and $V_{gs} > V_t$) and measure the degradation of linear region (low drain bias) threshold voltage and transconductance. Assessment of damage to the linear characteristics provides a worst-case view of total device degradation since CHE effects are not as pronounced in the saturation region [3]. Continuous stress of discrete FET's provides an accelerated measure of the reliability of FET's within a digital circuit. Since a typical "on" time of each circuit FET may be 3 percent of actual operating time [1], continuous stress of discrete FET's gives a fast reliability test (four months as opposed to 10 years). Recent results suggest that a pulsed stress of discrete devices may cause more degradation than the normal continuous stress [4]. This effect deserves further study. In this letter we consider the continuous stress only, but the measurement method we present is equally valid for all stress tests on discrete devices.

Continued constant field scaling to arbitrarily small channel lengths is not possible. For room temperature operation, the enhancement FET threshold should be greater than 0.5 V to avoid excessive drain current with the gate turned off. From circuit requirements, the power supply must be a factor of four times the threshold voltage [5]. Thus, the submicrometer device designer must contend with a minimum power supply of about 2 V. Given that today's 1.2-μm mask-length NMOS FET's are stable with respect to CHE degradation, with the aid of sidewall spacer technology [6] for 6-V power supplies, then first-order scaling [7] suggests that NMOS FET's with 0.4-μm mask length will be stable with a 2-V power supply. This argument shows that continued FET miniaturization (below 0.4 μm) coupled with subthreshold conduction and circuit requirements will necessitate our acceptance of increased CHE degradation.

Under this increased degradation we need to understand the effect of CHE stress on digital circuit performance. Switching delay time is a function of both linear and saturation FET characteristics. Thus, as stated previously, measurement of degradation to the linear characteristics only overstates the real damage to the digital delay time. We propose a simple I–V measurement and computation on a discrete NMOS FET that gives a realistic measure of the digital delay time. The ability to perform this measurement on discrete FET's preserves the advantage of continuous dc stress tests on discrete devices.

The role of the NMOS FET in digital switching is to discharge the drain (output) when the gate (input) switches above threshold. We model this situation by computing the time required for the NMOS FET, with a constant high gate voltage, to decrease the source–drain voltage from an initial high value to an arbitrary low value. Differentiating in time the charge stored on the drain

$$I_{ds}(V_{ds}) = C\frac{dV_{ds}}{dt} \quad (1)$$

where C is the drain capacitance. Thus, we see that the time (defined as τ) required to bring the output voltage down from an initial high level of V_{dd} to a low level of V_{do} is

$$\tau = C\int_{V_{do}}^{V_{dd}} dV_{ds}/I_{ds}(V_{ds}) \quad (2)$$

where we have assumed the drain capacitance is independent of drain bias.[1]

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[1] The assumption of constant capacitance is reasonable for the example we present since the capacitance is mostly due to external wiring. In practical applications, we should express the capacitance as the sum of depletion capacitances of the NMOS and PMOS drains and the gate–drain capacitance. This latter capacitance is fairly independent of bias [8].

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In formulating (1) and (2) we have made two idealizations. The first is the bias-independence of drain capacitance.[1] Second, we take the input waveform as being perfectly sharp (i.e., no switching delay in the input). In real circuit operation, however, the output of one stage may serve as the input of the following stage so that the input signal is not truly sharp as we have assumed. Incorporation of an arbitrary input waveform in (1) greatly complicates the analysis by introducing explicit time dependence and a closed-form solution is no longer possible. We are interested, however, in the fractional increase in digital switching time due to hot-electron stress and we do not expect this quantity to vary considerably with the shape of the input waveform.

To test the hypothesis that the above expression for delay time τ is an adequate measure of real digital circuit performance, we have conducted experiments with the simple CMOS inverter structure (with a 5-V power supply) depicted in Fig. 1. Fig. 2 shows a reproduction of an oscilloscope photograph of the portion of the inverter output controlled by the NMOS FET. The input frequency for all measurements is 200 kHz. Our inverter consists of individually bonded NMOS and PMOS FET's. Thus, the drain capacitance includes a parasitic component due to the external wiring. We measure I_{ds} versus V_{ds} (with V_{gs} fixed at the input pulse height) and perform the τ computation of (2) numerically with a Hewlett-Packard 9836 minicomputer interfaced to a Hewlett-Packard 4145 parameter analyzer.

Since the FET's of the inverter are discrete, we can subject them to high-voltage stress. We stressed both NMOS and PMOS devices for 100 h with 7 V on the gate and drain (negative bias on the PMOS). As expected, the CHE stress decreases the NMOS current drive and hence increases the switching delay time. Fig. 3 shows a direct oscilloscope measurement of the pre-stress and post-stress delay (with $V_{do} = 1$ V) versus input pulse height compared to the values predicted by our simple computation (solid line). The data points with error bars are the oscilloscope measurements. Note that our numerical integration for τ doesn't include the drain capacitance. We choose an appropriate capacitance (30 $\pm$ 1 pF for this externally wired inverter) to fit the pre-stress 3-V input pulse height measurement and assume that this capacitance is unchanged by the CHE stress. We add that different experimental configurations may possess different parasitic capacitances, but this is unimportant as long as the same experimental setup (with the same parasitic capacitance) is employed for both pre-stress and post-stress measurements. The agreement between direct oscilloscope measurement of the switching delay and that predicted by the measurement/computation of (2) on a discrete FET is good.

To obtain the data of Fig. 3, we stressed the NMOS FET in the *reverse* direction with respect to the source and drain terminals defined in Fig. 1. When we stress in the forward direction, we see virtually no degradation in the digital switching time as we have defined it here (2) even when there is considerable (40-percent) degradation in the linear region transconductance. Stressing in the reverse direction is more detrimental since this stress condition degrades the *I-V* characteristics of both the saturation and linear regions for forward mode operation.

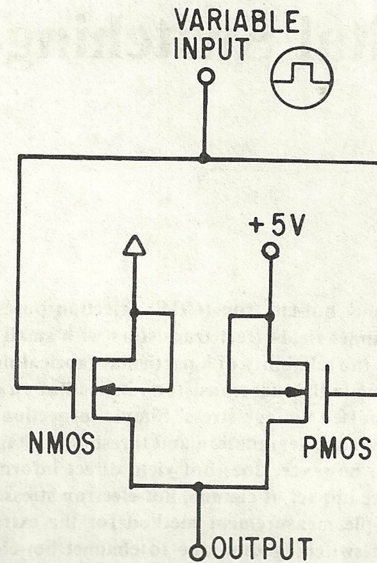

Fig. 1. Diagram of the CMOS inverter structure.

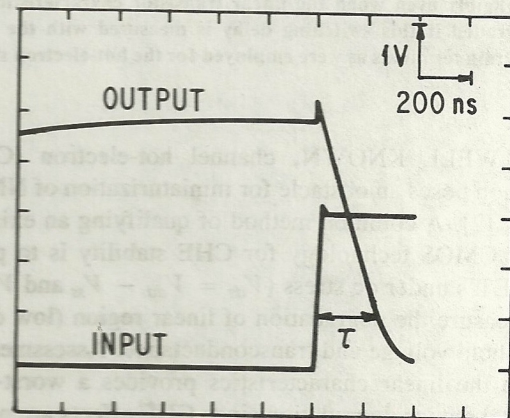

Fig. 2. Oscilloscope photograph of the input and output waveforms. In this picture, the input pulse height is 3 V. The portion of the inverter output controlled by the NMOS FET is shown after subjecting this FET to CHE stress. We define the delay as the time required for the output to fall to $V_{do} = 1$ V.

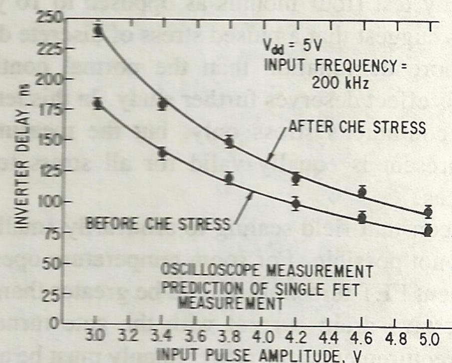

Fig. 3. Pre- and post-stress delay time measurements are shown as a function of input pulse height. The corresponding delay time computations based on a numerical integration of the *I-V* characteristics as discussed in the text are represented by the solid lines.

We have proposed a simple measurement technique to characterize a discrete FET before and after CHE stress. This measurement predicts well the relative increase in digital switching delay caused by CHE stress. We are now able to conduct accelerated reliability tests (by stressing discrete FET's) and monitor digital circuit performance degradation (increased switching time). As we commented earlier, either a continuous voltage stress or pulsed voltage stress [4] may be applied for the discrete FET stress. The advantage of this method over stressing an entire circuit lies in the observation that this latter stress is not accelerated (i.e., the FET's are only "on" 3 percent of the time). Also, our direct assessment of switching delay is more attuned to the reality of digital circuit degradation than simple inspection of linear FET characteristics in conventional discrete FET stress measurements.

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