Effect of Hot-Electron Stress on Low Frequency MOSFET Noise

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***Abstract*—Hot-electron reliability problems are of great importance in small geometry n-channel field-effect transistors. Accumulation of negative charge within the gate insulator and creation of interface states represent the two dominant degradation mechanisms. Since MOSFET noise is ascribed to Si-SiO$_2$ interface states, one might reasonably expect this noise to increase after hot-electron stress. We verify this expectation and show how the noise increase depends on gate voltage during stress. MOSFET noise is important for analog circuit performance and, hence, consideration of the long-term stability of noise, as well as threshold voltage and transconductance, should be included in analog circuit/process design.**

I. INTRODUCTION

ELECTRONS flowing from source to drain within an n-channel MOSFET gain energy from the electric-field component parallel to the electron flux. Decreasing the MOSFET gate length, in combination with the requisite increased channel doping, increases this electric field component and hence also increases the mean energy of the channel electrons. Device degradation arising from injection of channel electrons into the silicon dioxide gate insulator assumes increasing importance, therefore, as NMOSFET gate lengths decrease [1], [2].

This channel hot-electron (CHE) stress induces both oxide trapped charge and interface states [3]. Low-temperature subthreshold *I–V* [3] and charge-pumping current [4], [5] measurements have identified the creation of these surface states. The existence of these states has also been inferred from the FET damage annealing behavior [6]. In this letter we show measurements of increased MOSFET noise due to hot-electron stress and propose that this increased noise arises from interface states localized near the drain. This result has important ramifications for analog VLSI designs in which increased MOSFET noise may not be tolerable.

II. MEASUREMENTS

Conventionally fabricated NMOSFET's with nominal length and width values of 1.4 and 10 μm, respectively, served as the test vehicle for the noise measurements. Two boron implants define a p-well in the phosphorus-doped starting material and adjust the FET threshold voltage to ~0.5 V. Source and drain are implanted with arsenic and the gate material is phosphorus-diffused polycrystalline silicon.

We employ a Quan-Tech transistor noise analyzer to measure the MOSFET noise spectral density at discrete frequencies of 10, 10^2, 10^3, 10^4, and 10^5 Hz, before and after the hot-electron stress. We estimate a precision of ± 10 percent in these measurements. The source and p-well are held at ground potential while the drain is biased at 5 V and a constant current of 1 mA flows from source to drain. The gate bias is not fixed but adjusts itself to the level dictated by V_{ds} = 5 V and I_{ds} = 1mA. We then define the noise in terms of the equivalent fluctuations in gate voltage required to maintain the 1-mA drain current. For these devices, the mean gate bias (for V_{ds} = 5 V and I_{ds} = 1 mA), before hot-electron stress, is approximately 3 V so that we are measuring noise in the saturation (or pentode) regime. We operate the transistor, and hence obtain noise measurements, in both directions, by interchanging source and drain. This source–drain interchange should reveal asymmetry in the CHE degradation since the FET is characterized in saturation.

Grounding the source and p-well and applying a drain bias of 7 V for 60 min constitutes the hot-electron stress. After Takeda *et al.* [5], we vary the gate voltage during stress from 1 to 7 V in 2-V increments.

III. RESULTS AND DISCUSSION

Fig. 1(a)–(d) shows the noise spectral density as a function of frequency, before and after the CHE stress, with varying gate voltages during stress. The pre-stress noise values obtained by interchanging the source and drain are equivalent within the measurement precision and, therefore, we show only one pre-stress curve. Similarly, the forward post-stress noise is unchanged from its pre-stress value and hence is not explicitly shown in Fig. 1(a)–(d). The forward direction is defined such that the post-stress measurement is made with the same source and drain terminals as were used for the CHE stress. Reverse-direction measurements, on the other hand, treat the drain and source terminals of the CHE stress as the source and drain terminals for post-stress characterization, respectively.

We observe from Fig. 1(a)–(d) that CHE stress greatly increases MOSFET noise in the reverse direction but has little effect in the forward direction. This MOSFET noise is approximately proportional to $1/f$ (spectral density proportional to the inverse square root of frequency) and can, therefore, be attributed to surface states [7], [8]. Furthermore, in saturation the noise is dependent on the effective density of interface states near the source [9]. Thus given

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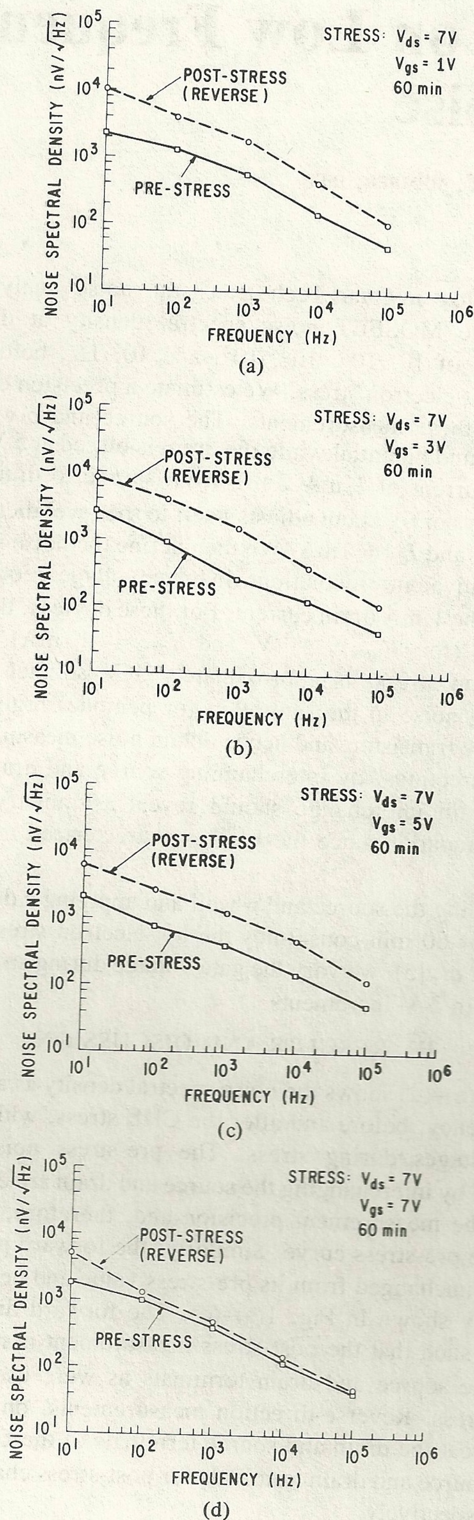

Fig. 1. (a)–(d) Noise spectral density is plotted versus frequency before and after a 60-min stress with V_{ds} = 7 V and V_{gs} = 1 V. The post-stress noise measurement is for reverse-mode operation.

these characteristics of $1/f$ noise and our results in Fig. 1(a)–(d), we conclude that CHE stress increases the surface-state density near the drain. We sketch this situation in Fig. 2(a) and (b). This conclusion is consistent with previous charge-pumping measurements [4], [5].

The smallest increase in MOSFET noise (and hence surface states) is observed for the highest gate voltage during stress. The greatest noise increase occurs with V_G = 3 V during stress although the V_G = 1 V condition is almost as severe. This gate voltage dependence is similar to the increased charge-pumping current observed by Takeda *et al.* [5].

Since all pre- and post-stress noise measurements are performed at V_{ds} = 5 V and I_{ds} = 1 mA, the nominal gate bias of each noise measurement is slightly different since hot-electron stress changes the FET I–V characteristics. For these stress conditions, the shift (increase) in this gate bias was always less than 0.3 V. On an unstressed FET, we varied the nominal gate bias over this interval (by adjusting the constant current I_{ds}) and found no effect on the measured noise within the measurement precision. Thus the increase in MOSFET noise after hot-electron stress is not due to the small change in FET operating point.

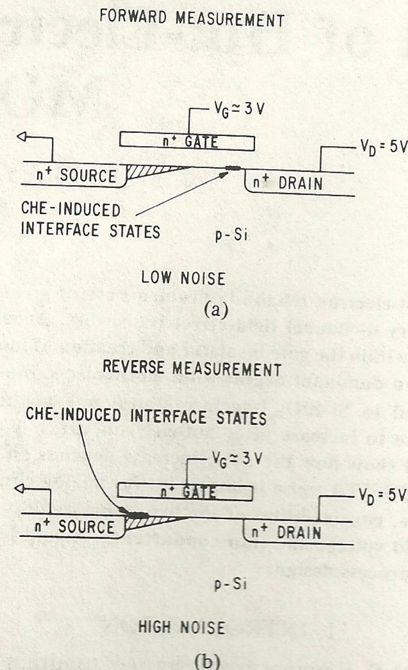

Fig. 2. (a) The noise measurement condition is sketched for the forward mode. (b) The noise measurement condition is sketched for the reverse mode.

IV. SUMMARY

We have measured increased MOSFET noise after CHE stress for reverse-mode operation. We conclude that CHE-induced surface states near the drain are responsible for this observation. The dependence of the noise increase on gate voltage during stress is consistent with earlier charge-pumping measurements. Analog circuit designs must include consideration of this increased MOSFET noise.

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REFERENCES

[1] T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schuster, and H.-N. Yu, "1 μm MOSFET VLSI technology: Part IV—Hot-electron design constraints," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 346–353, Apr. 1979.

[2] B. Eitan and D. Frohman-Bentchkowsky, "Hot-electron injection into the oxide in n-channel MOS devices," *IEEE Trans. Electron Devices,* vol. ED-28, pp. 328–340, Mar. 1981.

[3] T. H. Ning, C. M. Osburn, and H.-N. Yu, "Effect of electron trapping on IGFET characteristics," *J. Electron. Mater.*, vol. 6, no. 2, pp. 65–76, 1977.

[4] D. Schmitt and G. Dorda, "Interface states in MOSFET's due to hot-electron injection determined by the charge pumping technique," *Electron. Lett.*, vol. 17, no. 20, pp. 761–763, Oct. 1981.

[5] E. Takeda, A. Shimizu, and T. Hagiwara, "Role of hot-hole injection in hot-carrier effects and the small degraded channel region in MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 329–331, Sept. 1983.

[6] N. Shiono and C. Hashimoto, "Hot-electron limited operating voltages for 0.8-μm MOSFET's," *IEEE Trans. Electron Devices,* vol. ED-29, pp. 1630–1632, Oct. 1982.

[7] E. H. Nicollian and H. Melchior, "A quantitative theory of $1/f$ type noise due to interface states in thermally oxidized silicon," *Bell Syst. Tech. J.*, pp. 2019–2033, Nov. 1967.

[8] F. M. Klaasen, "Characterization of low $1/f$ noise in MOS transistors," *IEEE Trans. Electron Devices,* vol. ED-18, pp. 887–891, Oct. 1971.

[9] A. van der Ziel and K. Amberiadis, in *VLSI Electronics Microstructure Science*, vol. 7, N. Einspruch, Ed. pp. 261–302, 1983.

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