Comments on "Structure-Enhanced MOSFET Degradation Due to Hot-Electron Injection"

J. M. PIMBLEY AND G. GILDENBLAT, MEMBER, IEEE

Abstract—**Hsu and Grinolds recently compared channel hot-electron (CHE) stress results of conventional and "extended drain" NMOS FET's. [1]. They observe increasing degradation as the extended drain resistance increases when the drain bias is defined as that which produces a fixed substrate current. A model in which the hot-electron stress induces surface states within the extended drain region is proposed. We argue that the drain bias condition chosen for these measurements does not produce equal numbers of channel hot electrons in all devices as is claimed. Since the ratio of substrate current to source current is a measure of the mean electron energy, we claim that this ratio (and hence the mean electron energy) increases as extended drain resistance increases.**

IN A RECENT LETTER, Hsu and Grinolds compared the channel hot-electron (CHE) degradation rates of NMOS field-effect transistors fabricated with several different source/drain doping processes [1]. These doping processes included the conventional method in which the gate serves as a self-aligned mask for the high dose n^+ ion implant as well as other extended drain (nonoverlap gate and lightly doped drain) methods which tend to decrease electric field strength within the device and increase the effective channel length. Hsu and Grinolds found that when each type of device is biased such that the substrate currents are equal, the conventionally fabricated FET exhibits the greatest resistance to CHE degradation. Thus a new and valuable empirical assessment of the increase in CHE reliability due to processing and design innovations (such as the extended drain) is born. By equating substrate currents in two dissimilar NMOS FET's, one quickly determines an upper limit to the difference in maximum applicable drain voltages between the two devices. This upper limit is just the drain voltage difference required to equilibrate the substrate current in the two devices.

Manuscript received April 13, 1984.

The authors are with the General Electric Corporate Research and Development Center, Schenectady, NY 12301.

Hsu and Grinolds claim that interface state generation near the drain is responsible for the observed CHE degradation. The argument continues that as the drain series resistance increases (as it does with nonconventional device structures), the negatively charged surface states deplete more of the extended drain region and greater CHE degradation is observed. The two-dimensional nature of current flow and electrostatic potential distribution within the FET, coupled with a spatially nonuniform surface state distribution, render further investigation of this model fairly difficult.

In our opinion, the initial presumption that equivalent CHE damage is inflicted in all devices is incorrect. Hsu and Grinolds make the excellent observation that when two NMOS FET's are biased differently but produce the same substrate current, then the numbers of "hot" electrons in the channel of each device are equal. This statement reflects the nature of the avalanche ionization mechanism that produces the substrate current [2], [3]. More precisely, then, the numbers of electrons in the channel of each device with sufficient energy (~1.7 eV) to generate an electron-hole pair by avalanche ionization are equal.

The ratio of substrate and source currents (I_x/I_s) yields a measure of the maximum field strength parallel to the current flow [3]. Thus when the substrate currents of two devices are equilibrated (by adjusting the relative drain bias), the device with highest source current will possess a smaller I_x/I_s ratio and hence a smaller maximum field. Clearly, the conventionally fabricated device will have the highest source current since, of all devices compared in the Hsu-Grinolds experiment, this FET has the smallest effective channel length [4]. A lower maximum field implies a lower maximum electron temperature in the quasi-thermal equilibrium model of CHE injection [5]. As electron temperature decreases, the rate of decline with energy of the quantity $n(E)dE$, which describes the density of channel electrons with energy between E and $E + dE$,

0741-3106/84/0700-0256$01.00 © 1984 IEEE

increases. Since the areas under two curves from $E \sim 1.7$ eV (available injection threshold) to infinite energy are equal for equal substrate currents, the areas under these same curves from some higher lower limit (such as the 3.2-eV Si–SiO_2 barrier height) to infinity will differ for different electron temperatures. In particular, the lower electron temperature device will have a smaller integrated electron energy distribution function than the higher electron temperature device. We show this situation in Fig. 1 [6]. In other words, the device with lower source current (higher electron temperature) when substrate currents are equal will contain more "hot" electrons when "hot" electrons are defined to have energy greater than, say, 3.2 eV.

It is now clear why the conventional devices of Hsu and Grinolds suffered the least CHE degradation of those tested. This device had the least number of electrons capable of surmounting the Si–SiO_2 energy barrier. Note that interface states are generated by electrons injected over this barrier [7], [8]. The CHE degradation rate dependence on n^- region sheet resistance is now revealed. As this resistance increases, the source current obtained at the target substrate current value decreases [4]. Thus the ratio I_x/I_s, and hence the maximum electric field and electron temperature, increases. We claim, therefore, that more CHE damage occurs as n^- resistance increases (and substrate current is equilibrated by increasing the drain voltage). This concept contradicts the model of Hsu and Grinolds. In this latter model, the CHE damage is claimed to be equivalent for all devices but has greater influence on the device I-V characteristics as the n^- resistance increases.

To illustrate our ideas more clearly, we cite the following gedanken experiment. Suppose we have a 1-μm effective channel length NMOS FET with $V_{gs} = 3$ V and $V_{ds} = 6$ V. We compare this device under these bias conditions with a 2-μm effective channel length NMOS FET with $V_{gs} = 3$ V. We adjust the drain bias of the longer channel device to the value (>6 V) which yields the same substrate current as is observed in the shorter channel FET. The source current in the longer FET will be smaller than in the shorter FET due to the W/L factor of the FET I-V characteristic and the fact that these devices are operated in the saturation region. Hence, we claim that the maximum field will be greatest in the longer FET under these bias conditions (different drain voltages). The CHE degradation will also be greater in the longer device. Yet the conclusion that the shorter FET is more stable under CHE stress than the longer FET is somewhat paradoxical. One must question the validity of comparing these two devices at these differing bias conditions.

Hsu and Grinolds also remark on the qualitative differences between post-stress linear transconductance curves plotted versus gate bias. Specifically, the post-stress transconductance does not approach the pre-stress value at high gate bias for the LDD FET as it does for the conventional FET. This characteristic of the LDD FET is interpreted as evidence of carrier depletion within the LDD n^- region due to CHE-induced surface states. In Fig. 2(a) and (b) we show pre- and post-stress linear transconductance plotted versus gate bias for two stress conditions with LDD NMOS FET's fabricated with an oxide sidewall spacer source/drain doping process [8]. We note that in

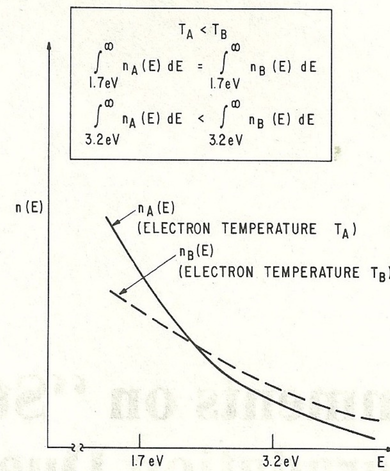
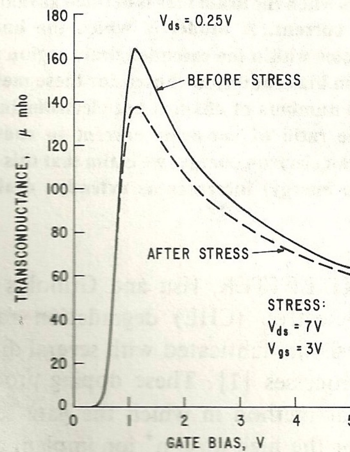
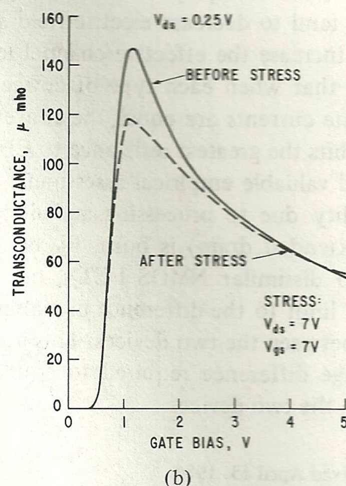


Fig. 1. The conduction electron density per unit energy is sketched as a function of energy for two different electron temperatures (T_A and T_B). The integral of these two distributions from the avalanche ionization threshold energy to infinity are equal by definition since the substrate currents are equilibrated. This condition necessarily implies that, with $T_A < T_B$, the integral of these same curves from a higher energy (here, 3.2 eV) to infinity obey the inequality shown.



(a)



(b)

Fig. 2. Short channel LDD NMOS FET, linear region ($V_{ds} = 0.25$ V) transconductance is plotted versus gate bias (a) before and (b) after stress for two conditions.

the $V_{gs} = V_{ds}$ stress, the transconductance curve is not of the form required by the surface-state degradation model of Hsu and Grinolds.

REFERENCES

[1] F.-C. Hsu and H. R. Grinolds, "Structure-enhanced MOSFET degradation due to hot-electron injection," *IEEE Electron Device Lett.*, vol. EDL-5, p. 71, Mar. 1984.

[2] S. Abbas, "Substrate current—A device and process monitor," in *IEDM Tech. Dig.*, 1974, p. 404.

[3] R. R. Troutman, "Low-level avalanche multiplication in IGFET's," *IEEE Trans. Electron Devices*, vol. ED-23, p. 419, Apr. 1976.

[4] This statement rests on the assumption that the substrate currents are equilibrated by adjusing the drain bias only and not the gate bias. Also, we require the FET to be in saturation so that increasing the drain bias raises the source current negligibly. These conditions are consistent with the technique of Hsu and Grinolds.

[5] E. Takeda, H. Kume, T. Toyabe, and S. Asai, "Submicrometer MOSFET structure for minimizing hot-carrier generation," vol. SC-17, p. 241, 1982.

[6] Actually, we need not restrict the electron energy distribution function to be Maxwellian in the preceding argument as is the case with the quasi-thermal equilibrium model. As long as $n(E)$ is monotonically decreasing above 1.7 eV and a greater maximum electric field implies a smaller rate of decline of $n(E)$ with energy, equating the integrals of two distributions from $E \sim 1.7$ eV to infinity still yields the same inequality between integrals of the same distributions from any other integration limit greater than 1.7 eV.

[7] S. K. Lai and D. R. Young, "Effects of avalanche injection of electrons into silicon dioxide—Generation of fast and slow interface states," *J. Appl. Phys.*, vol. 52, no. 10, p. 6231, 1981

[8] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, "Characterization of simultaneous bulk and interface high-field trapping effects in SiO_2," in *IEDM Tech. Dig.*, 1983, p. 182.

[9] P. J. Tsang, S. Ogura, W. W. Walker, J. F. Shepard, and D. L. Critchlow, "Fabrication of high-performance LDDFET's with oxide sidewall-spacer technology," *IEEE Trans. Electron Devices*, vol. ED-29, p. 590, 1982.

0741-3106/84/0700-0258$01.00 © 1984 IEEE